We claim:

1. A test structure in a test area of a semiconductor substrate for measuring a parasitic inductance in an integrated circuit fabricated on the semiconductor substrate, comprising:

an LC oscillator circuit;

at least one substructure in the LC oscillator circuit and including a circuit element having a same layout as a circuit element in the integrated circuit contributing the parasitic inductance; and

at least one varactor having a capacitance adjustable by a control voltage source; and

wherein when the varactor is adjusted to a certain capacitance value, a stable oscillation can be generated in the LC oscillator circuit, and a frequency of the oscillation is dependent on an inductance associated with the substructure, which is related to the parasitic inductance in the integrated circuit.

2. The test structure of claim 1 wherein the integrated circuit includes a first interconnect line and the substructure includes a second interconnect line having a same layout on the semiconductor wafer as the first interconnect line.

3. The test structure of claim 1 wherein the integrated circuit includes a first via and the substructure includes a second via having a same layout on the semiconductor wafer as the first via.

4. The test structure of claim 1 wherein the integrated circuit includes a first diffusion region and the substructure includes a second diffusion region having a same layout on the semiconductor wafer as the first diffusion region.

5. The test structure of claim 1 wherein the substructure is one of a pair of substructures that are laid out on the semiconductor wafer such that they are mirror images of each other.

6. The test structure of claim 5 wherein the varactor is one of a pair of varactors that are laid out on the semiconductor wafer such that they are mirror images of each other.

7. The test structure of claim 6 wherein the pair of substructures and the pair of varactors together form an LC tank of the LC oscillator circuit .

8. The test structure of claim 7, further comprising a pair of P-type transistors and a pair of N-type transistors that are part of the LC oscillator circuit.

9. The test structure of claim 8, wherein the P-type transistors and N-type transistors together contribute a negative resistance that cancels an equivalent parallel resistance of the LC tank.

10. The test structure of claim 1 wherein the LC oscillator circuit is laid out symmetrically on the semiconductor substrate such that one half of it is a mirror image of another half.

11. The test structure of claim 1, further comprising:

a frequency divider connected to the LC oscillator circuit.

12. The test structure of claim 11, further comprising:

a buffer connected to the frequency divider; and

a pad connected to the buffer for connecting the test structure to a frequency meter.

13. A method for measuring a parasitic inductance in an integrated circuit fabricated on a semiconductor substrate, comprising:

selecting a test chip on the semiconductor substrate, the test chip including a circuit element having a same layout as a circuit element in the integrated circuit that contributes the parasitic inductance;

applying a control voltage to the test chip and adjusting the control voltage until a stable oscillation is generated in the test chip;

measuring a frequency of the oscillation; and

determining the parasitic inductance using the frequency.

14. The method of claim 13 wherein the test chip includes an LC oscillator circuit and determining the parasitic inductance using the frequency comprises:

deriving a relationship between the frequency and capacitances and inductances in the LC oscillator circuit;

determining the values of the capacitances; and

determining the parasitic inductance based on the relationship and the values of the capacitances.

15. The method of claim 14 wherein deriving a relationship between the frequency and capacitances and inductances in the LC oscillator circuit comprises simulating the LC oscillator circuit to obtain the relationship.

16. The method of claim 14 wherein the LC oscillator circuit includes at least one varactor and determining the values of the capacitances comprises determining the capacitance of the varactor based on the control voltage at which the stable oscillation is generated in the test chip.

17. The method of claim 14 wherein determining the values of the capacitance comprises measuring parasitic capacitances in the LC oscillator circuit.

18. A test structure in a test area adjacent at least one integrated circuit on a semiconductor wafer, the test structure comprising an LC oscillator circuit having an oscillation frequency related to a parasitic inductance associated with a subcircuit in the at least one integrated circuit.

19. The test structure of claim 18 wherein the test structure further comprises at least one substructure in the LC oscillator circuit, the substructure having a same layout as the subcircuit contributing the parasitic inductance.

20. The test structure of claim 18 wherein the test structure further comprises at least one varactor having an adjustable capacitance related to the oscillation frequency.